CLAIMS

1. An apparatus for regenerating reset and clock signals, comprising:

a clock circuit for receiving an external clock signal and generating therefrom an internal clock signal, the internal clock signal being forwarded to a plurality of clocked circuits to clock the clocked circuits;

a reset circuit for receiving an external reset signal and generating therefrom an internal reset signal, the internal reset signal being forwarded to the plurality of clocked circuits to reset the clocked circuits; and

a clock masking circuit for masking the internal clock signal for a masking period such that the clocked circuits are not clocked during the masking period.

2. The apparatus of claim 1, wherein the reset circuit generates the internal reset signal in a transition to an inactive state during the masking period.

3. The apparatus of claim 2, wherein the internal reset signal transitions to an inactive state at a substantial midpoint of the masking period.

4. The apparatus of claim 1, further comprising a counter circuit for generating a count of a number of cycles of the external clock signal.

5. The apparatus of claim 4, further comprising a first comparator circuit for comparing the count with a first threshold and initiating the masking period when the count reaches the first threshold.

6. The apparatus of claim 5, further comprising a second comparator circuit for comparing the count with a second threshold and terminating the masking period when the count reaches the second threshold.

7. The apparatus of claim 6, further comprising a third comparator circuit for comparing the count with a third threshold and transitioning the internal reset signal to an inactive state when the count reaches the third threshold.

8. The apparatus of claim 7, wherein the third threshold is between the first and second thresholds.

9. The apparatus of claim 7, wherein the third threshold is substantially midway between the first and second thresholds.

10. The apparatus of claim 7, wherein the first, second and third thresholds are selected such that, in all of the clocked circuits, ambiguity with respect to timing of clocking and resetting the clocked circuits is eliminated.

11. The apparatus of claim 1, further comprising a mask delay circuit for delaying the masking period until after an active-to-inactive transition of the internal clock signal.

12. The apparatus of claim 1, further comprising a mask delay circuit for delaying the masking period until after a predicted external clock signal routing delay.

13. The apparatus of claim 1, wherein the clocked circuits are flip-flops.

14. The apparatus of claim 1, wherein the clocked circuits are D flip-flops.

15. The apparatus of claim 1, wherein the masking circuit generates a mask signal used in initiating and terminating the masking period.

16. A method for regenerating reset and clock signals, comprising:

receiving an external reset signal;

receiving an external clock signal;

generating from the external reset signal an internal reset signal, the internal reset signal being forwarded to the plurality of clocked circuits to reset the clocked circuits;

generating from the external clock signal an internal clock signal, the internal clock signal being forwarded to a plurality of clocked circuits to clock the clocked circuits; and

masking the internal clock signal for a masking period such that the clocked circuits are not clocked during the masking period.

17. The method of claim 16, further comprising generating the internal reset signal in a transition to an inactive state during the masking period.

18. The method of claim 17, wherein the internal reset signal transitions to an inactive state at a substantial midpoint of the masking period.

19. The method of claim 16, further comprising generating a count of a number of cycles of the external clock signal.

20. The method of claim 19, further comprising comparing the count with a first threshold and initiating the masking period when the count reaches the first threshold.

21. The method of claim 20, further comprising comparing the count with a second threshold and terminating the masking period when the count reaches the second threshold.

22. The method of claim 21, further comprising comparing the count with a third threshold and transitioning the internal reset signal to an inactive state when the count reaches the third threshold.

23. The method of claim 22, wherein the third threshold is between the first and second thresholds.

24. The method of claim 22, wherein the third threshold is substantially midway between the first and second thresholds.

25. The method of claim 22, wherein the first, second and third thresholds are selected such that, in all of the clocked circuits, ambiguity with respect to timing of clocking and resetting the clocked circuits is eliminated.

26. The method of claim 16, further comprising delaying the masking period until after an active-to-inactive transition of the internal clock signal.

27. The method of claim 16, further comprising delaying the masking period until after a predicted external clock signal routing delay.

28. The method of claim 16, wherein the clocked circuits are flip-flops.

29. The method of claim 16, wherein the clocked circuits are D flip-flops.

30. The method of claim 16, further comprising generating a mask signal used in initiating and terminating the masking period.

31. A high-speed digital system, comprising:

a plurality of function blocks;

a bus to which the function blocks are coupled; and

a reset signal and clock signal regenerating circuit comprising:

a clock circuit for receiving an external clock signal and generating therefrom an internal clock signal, the internal clock signal being forwarded to a plurality of clocked circuits to clock the clocked circuits,

a reset circuit for receiving an external reset signal and generating therefrom an internal reset signal, the internal reset signal being forwarded to the plurality of clocked circuits to reset the clocked circuits, and

a clock masking circuit for masking the internal clock signal for a masking period such that the clocked circuits are not clocked during the masking period.

32. The system of claim 31, wherein the reset circuit generates the internal reset signal in a transition to an inactive state during the masking period.

33. The system of claim 32, wherein the internal reset signal transitions to an inactive state at a substantial midpoint of the masking period.

34. The system of claim 31, further comprising a counter circuit for generating a count of a number of cycles of the external clock signal.

35. The system of claim 34, further comprising a first comparator circuit for comparing the count with a first threshold and initiating the masking period when the count reaches the first threshold.

36. The system of claim 35, further comprising a second comparator circuit for comparing the count with a second threshold and terminating the masking period when the count reaches the second threshold.

37. The system of claim 36, further comprising a third comparator circuit for comparing the count with a third threshold and transitioning the internal reset signal to an inactive state when the count reaches the third threshold.

38. The system of claim 37, wherein the third threshold is between the first and second thresholds.

39. The system of claim 37, wherein the third threshold is substantially midway between the first and second thresholds.

40. The system of claim 37, wherein the first, second and third thresholds are selected such that, in all of the clocked circuits, ambiguity with respect to timing of clocking and resetting the clocked circuits is eliminated.

41. The system of claim 31, further comprising a mask delay circuit for delaying the masking period until after an active-to-inactive transition of the internal clock signal.

42. The system of claim 31, further comprising a mask delay circuit for delaying the masking period until after a predicted external clock signal routing delay.

43. The system of claim 41, wherein the clocked circuits are flip-flops.

44. The system of claim 41, wherein the clocked circuits are D flip-flops.

45. The system of claim 41, wherein the masking circuit generates a mask signal used in initiating and terminating the masking period.